SEE and TID Extension Testing of the Xilinx XQR18V04 4Mbit Radiation Hardened Configuration PROM

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Abstract

The XQR18V04 was evaluated for single event upset rates using proton and heavy ions. The PROM was demonstrated to be immune to latch-up, as well as to static upset in the flash memory cells, to an LET > 125 MeV/mg/cm^2 (effective). The PROM was also tested in a dynamic mode, which revealed three distinct error modes: Read Bit Errors, Address Errors, and a Single Event Functional Interrupt (SEFI) which affected the data output drivers. Saturation cross-sections, and onset thresholds, for these error modes were measured at the heavy ion facility at Texas A&M University, and the proton facility at UC Davis. Additional testing was performed at UC Davis and the Cobalt 60 source at McClellan Air Force Base to examine the effect to TID life as a function of power biasing. The PROM demonstrated a 100% improvement in total TID life with an 84% percent decrease in device usage.

I. Introduction

The Xilinx *XQR18V04* Configuration PROM is an ISP (In System Programmable) 4 Mbit flash memory device that is primarily used to store Xilinx FPGA configuration data. The ability to reprogram the device remotely while in operation makes it especially favorable for use with FPGAs in space and avionic applications. Due to the architecture of FPGAs, the many static configuration memory cells are susceptible to single event upsets that can lead to functional errors. Therefore, FPGA configuration memory content requires frequent refresh. This configuration PROM also supports a byte-wide output format that is compatible with FPGA configuration "scrubbing" (background auto-refresh of the FPGA's configuration memory). Although the flash memory cells are themselves not susceptible to static upset, the CMOS circuitry used to decode and read out the stored data are susceptible to transient as well as static upsets. Several test vehicles were developed to exercise an XQR18V04 as it would be used for FPGA configuration operations in order to capture and analyze any possible error mode exhibited. Single event upset and total ionizing dose experiments were conducted using heavy ions at the Texas A&M cyclotron, protons at the UC Davis cyclotron, and gamma ray from a Co60 source at McClellan Air Force Base.

II. Experimental Details

A. Device Properties

The XQR18V04 contains 4,194,304 non-volatile flash memory cells that are programmed and erased from an IEEE 1149.1 boundary-scan (JTAG) interface. The flash memory array is addressed with an internal counter (*Address Counter*). The addressed memory data is accessed, decoded and output in either a single bit or eight bit wide format which is determined when the PROM is programmed. The external input pin RST/OE is an active low reset to the internal address counter and an active high enable for the data output drivers. When RST/OE is asserted low, the address counter is returned to a value of zero (0x000000) which addresses the first (8 bit) memory address. When RST/OE is then asserted back high the data output pins (D0:D7) display the current memory address contents. When CE (clock enable) is asserted high, each rising edge of the CLK pin (clock input) will increment the address counter by one and the new memory address contents will show up on the output data lines. When the address counter has reached it's terminal count (maximum address value) the data output drivers are disabled and the external output pin CEO (Clock Enable Out) is asserted low by the PROM.

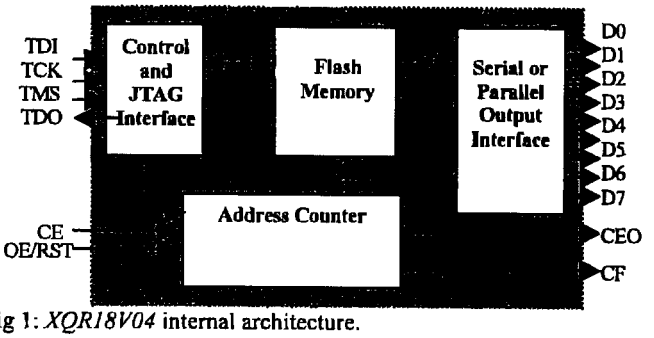

Fig 1: *XQR18V04* internal architecture.

The device chosen for this study, the radiation hardened XQR18V04PC44, is the same mask design as the commercial device, XC18V04, except that it is fabricated on epitaxial silicon wafer for latch-up resistance. Device was procured as an engineering sample in a 44-pin wire-bond standard plastic leaded chip carrier (PLCC) package so that the plastic package molding compounds could be etched off to expose the top of the die. The XQR18V04 is fabricated on a 0.33µm low power CMOS/Flash process

with a 3.3 V core operation voltage and 8 V internal charge pumps for programming. The devices were chemically etched at the Xilinx Failure Analysis Laboratory to expose the die and help improve ion range.

B. Irradiation Facilities

Heavy ion irradiation tests were performed at the Cyclotron Institute's Radiation Effects Facility at Texas A & M University in College Station, Texas. Their facility consists of a set of high energy (25 MeV/nucleon) noble gas beams (Ne, Ar, Kr, and Xe) that provides a broad range of linear energy transfer (LET) (2-63 MeV/(mg/cm^2)) and range penetration (254 to 790 microns). The ions used for this experiment are Neon, Argon, Krypton, and Xenon to obtain LETs from 1.21 – 61.3 MeV/(mg/cm^2). All tests were performed in air with a layer definition file put in.

Proton irradiation tests were performed at the Crocker Nuclear Facility at the University of California in Davis, California. The facility provided a proton beam at an energy level of 63 MeV, and range of beam currents (10 pA to 10 nA) in order to precisely control the particle flux densities. Due to the range of high-energy protons and the nature of their interactions, all tests were performed in air and etched parts were not necessary for this experiment.

Gamma irradiation tests were performed using the Cobalt 60 source at the Centre for Defense MicroElectronics Activity (DMEA) in McClellan Park (formerly McClellan Air Force Base) Sacramento, CA. The high dose irradiator has a curie content of 19,200 Co_{60}, and provided a dose rate of 50 rad(SiO_2)/sec.

C. Test Procedure

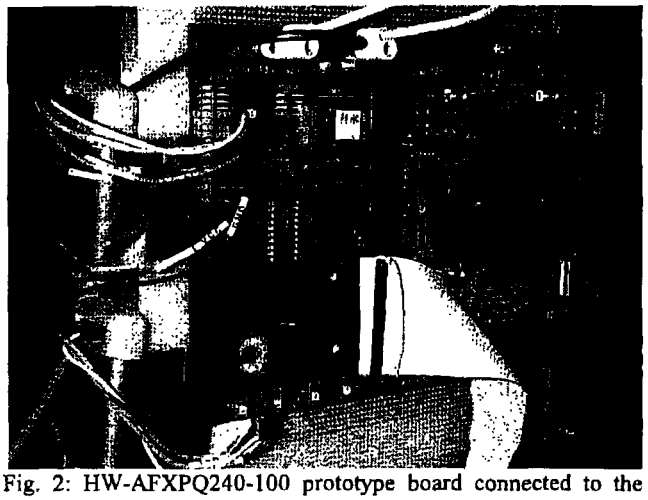

Fig. 2: HW-AFXPQ240-100 prototype board connected to the host PC and test software via two Xilinx Parallel Cable III connectors and a custom hardware controller via a 40 wire ribbon cable.

The SEU and extended TID characterization of XQR18V04 is composed of data collected from four different static and dynamic tests conducted at the three fore-mentioned facilities. They are a static memory and latch-up test conducted with heavy ion, dynamic function test with proton and heavy ion, and a static unbiased total dose test with gamma rays. The test vehicle is shown in figure 2.

1) Static Memory and Latch-Up Test

This test comprised of extracting only memory bit upsets using Xilinx IMPACT device programming application to program and verify the device through one of the parallel III JTAG IEEE 1149.1 interface cables (see figure 2). The PROM was preprogrammed before the experiment with a known test pattern. Immediately following each beam run, the 'verify' function was performed, with the IMPACT application software, to determine the number of differences in the flash memory array.

2) Dynamic Function Test

The dynamic function test uses an FPGA (XCV300PQ240) to observe the output of two identical XQR18V04 devices. A diagram of the test setup is shown in figure 3.

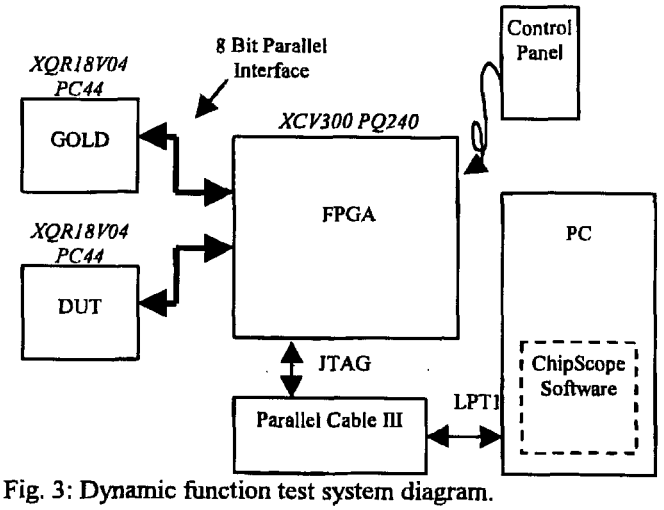

Fig. 3: Dynamic function test system diagram.

The FPGA runs an automated series of tests on both PROMs. Only one of the two PROMs are irradiated. When differences between the two PROMs are observed, the nature of the error is analyzed for expected error signatures. The expected error signatures are *Data Errors*, *Address Errors*, *CEO Error*, *Stuck-at-0*, *Stuck-at-1*, and *Power-Cycle*. When an error signature is recognized, an associated counter within the FPGA design is incremented. The test runs repeatedly until halted by the user. At the end of each beam run the automated test program is halted and the result of the error counters are uploaded to the host PC through the other Parallel Cable III using the Xilinx "ChipScope ILA" application software. The ChipScope ILA software was designed as an Internal Logic Analyzer for Virtex Series FPGA designs. The ILA units are connected to their associated counters as shown in figure 4.

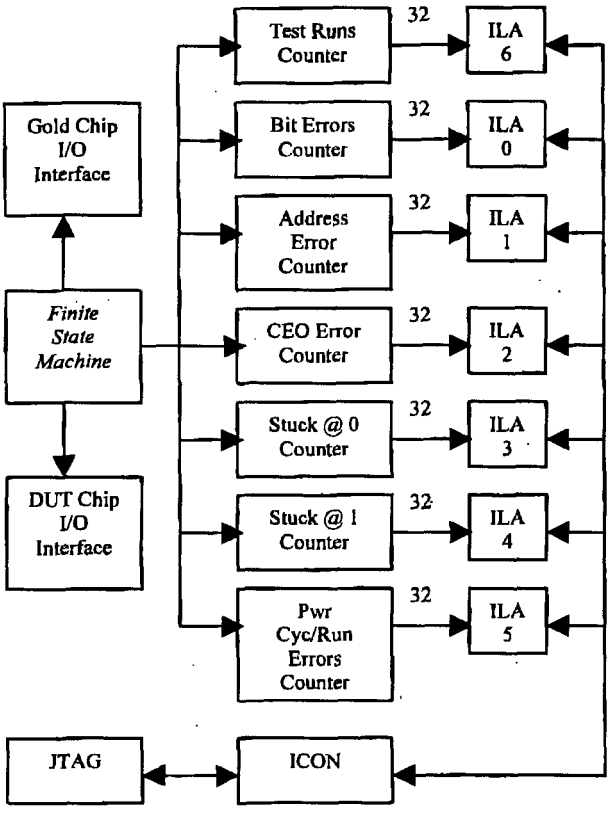

Fig. 4: Control chip (FPGA) architecture.

A finite state machine was implemented to carry out the test flow shown in figure 5. The test begins with an initialization of the two PROMs by asserting their reset pins (RST/OE). The two devices are enabled and clocked until either device lowers it CEO output pin. While the devices are being clocked the 8 bit data output ports of each device are compared for discrepancies. A running count of individual data bit mismatches are accumulated and stored in a temporary register. If both devices lower their CEO pins at the same time, all recorded data errors are considered to be true errors and the tally for the current run is added to the master data error counter and the run resets. If the CEO of the DUT arrives either early or late then it is either the result of an address error or an upset to the CEO itself. If a CEO error is accompanied by a large number of data errors, then the error signature is recognized as an address error, rather than a CEO error, and the data read errors are disregarded. If the CEO error is not accompanied by a large number of data read errors, then it is considered to be an error in the CEO itself. If following the first data error the data output becomes stuck at either 1 or 0, then a 'stuck bits' test is performed. If a possible stuck bit condition is observed it is noted in a temporary register and the DUT is reset and tested again. If the stuck condition does not persist then the previous run is noted as a stuck bit error (either 1 or 0). If the stuck bit condition does persist, however, then this is also noted in a temporary register and the DUT is power-cycled and re-tested. If the power-cycle recovers the DUT from the stuck condition, then this is noted in the power-cycle counter and a new test iteration begins. However, if power cycling does not recover the DUT, then human intervention is required.

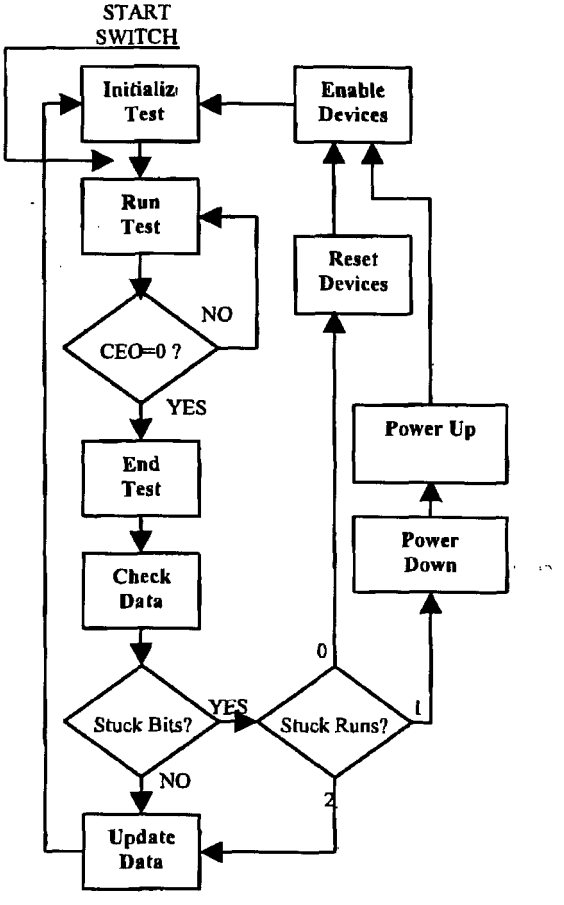

Fig. 5: Test flow chart.

3) Unbiased extended TID testing

The XQR18V04 has a specified TID life of 40 krad(Si). A method of improving this to match the companion FPGAs which have a rated TID life of 100~300 krad(Si) is required. Since configuration PROMs are not in constant use in any system, the TID benefits of not biasing the PROMs when not in use, can be used to match the TID life of the PROM and the FPGA. Two tests were conducted to evaluate the benefit to TID life expectancy by introducing periods of non-biasing to a PROM in an application or system. The first test was conducted using gamma ray from a cobalt 60 source to test the maximum TID life of an un-biased PROM. The second test was conducted with protons during the dynamic functional test.

For the gamma test, ten samples were dosed in three different bias configurations (shown in table 1). Samples were pulled and tested at 100 krad, 200 krad, and 300 krad. The dose rate used for this experiment was 3.6

krad(Si)/min. Testing was performed on site without annealing. The test steps are as follows:

1. Read JTAG Vendor ID code.
2. Program PROM with Configuration Bitstream
3. Verify program data.
4. Configure XCV300 with PROM in Master Serial Mode.

Table 1: Non-biasing conditions tested

Configuration	Biasing Condition	Samples
1	VCC, Clock, No GND	2
2	GND, Clock, No VCC	4
3	GND, No Clock, No VCC	4

The proton test was conducted by modifying the dynamic function test to always power-cycle the DUT between test runs. The length of time that the DUT was left un-powered between test runs was selected such that the total time that the DUT was powered in the beam was only 16% of the total time that the DUT was in the beam. Two tests were conducted each until the PROM was functionally failing due to TID effects.

III. Test Results

The results of each experiment are summarized in the following sections.

A. Static Memory and Latch-Up Test

The PROM was tested with Au ion up to an LET of 119 MeV/cm2/mg for a fluence greater than 1E7 particles/cm^2. Table 2 shows a complete listing of the test runs. After each test run the PROM memory content was verified using the IMPACT software. No bit upsets occurred in the PROM's memory and there were no indications of any latch-up conditions. The entire experiment was performed without removing power from the PROM.

Table 2: Static Test Runs

LET	Species	Angle	Fluence	Bit Errors
83	Au	0	1.00E+05	0
83	Au	0	1.00E+05	0
83	Au	0	1.00E+05	0
83	Au	0	1.00E+05	0
83	Au	0	1.00E+05	0
83	Au	0	1.00E+07	0
119	Au	45	1.00E+07	0

B. Dynamic Functional Test

The dynamic functional test was first performed with 63 MeV protons at a flux of 8.7E8 (p/cm^2/s). Due to the small cross-sections of the error modes and the high ionizing dose rate from the proton interactions only a limited data set was obtained with the available facility time. The results are shown in table 3.

Two samples were tested ~~were tested~~ for three runs each. For each sample, the PROM ceased functioning during the third run due to accumulated total ionizing dose effects. Thus, no SEU data was obtained for the third run of each sample. From the two runs on the first sample one Address Error was recorded. From the two runs on the second sample three Bit Errors were observed. No stuck bit conditions or CEO errors were observed.

Table 3: Proton test results for dynamic function test.

Sample (SN)	Fluence (p/cm^2/s)	Dose (krad, accum)	Runs	Bit Error	ADDR Error
1	2.60E+11	39.1	529	0	0
1	2.60E+11	74.2	587	0	1
2	2.90E+11	40.0	616	3	0
2	2.90E+11	80.0	617	0	0

The test was next performed with a 25MeV/nucleon noble gas heavy ion beam. Again, Data Errors and Address Errors were observed, but no stuck bit conditions or CEO errors were observed. However, a new error mode was observed which has been categorized as a SEFI (Single Event Functional Interupt). The signature of the SEFI mode was such that a sudden large number of data errors (500,000–4,000,000) were observed on a single test run. Ordinarily, this would indicate an address error except that the CEO transitioned at the same time as the comparison device. This indicates that the address counter was not upset. The possibility that this error mode was causing an internal reset was considered. However, it's assumed that such a reset would also effect the CEO timing. Our current assumption is that this error mode caused the output drivers to be disabled. Since subsequent test runs within the same beam run produced expected results, this SEFI mode is recoverable by simply asserting the reset (RST/OE). The collected data for the various error modes are shown in the following figures. The Weibull function was used to fit the data according to the equation:

$$F(L) = \acute{o}_{sat}\,(1 - \exp\{-[(L-L_0)/W]^s\})$$

where:

F(L)	= SEU cross-section in i^2/bit;
$\acute{o}_{sat}$	= saturation cross-section;
L	= effective LET in MeV-cm^2/mg;
L_0	= upset threshold LET;
W	= width parameter;
s	= a dimensionless exponent.

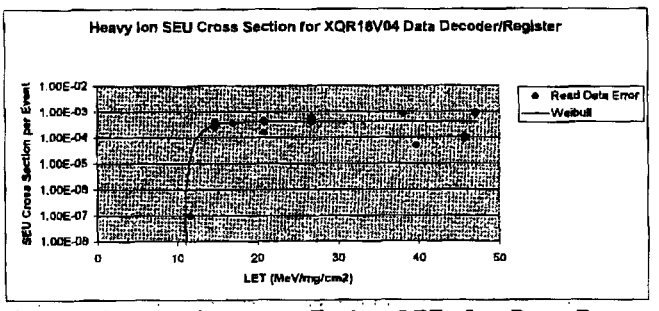

Fig. 6: Cross-section vs. effective LET for Data Errors. Saturation cross-section (σ_{sat}) is 4.5E-5 cm^2/device and L_0 is 11.0 MeVcm^2/mg.

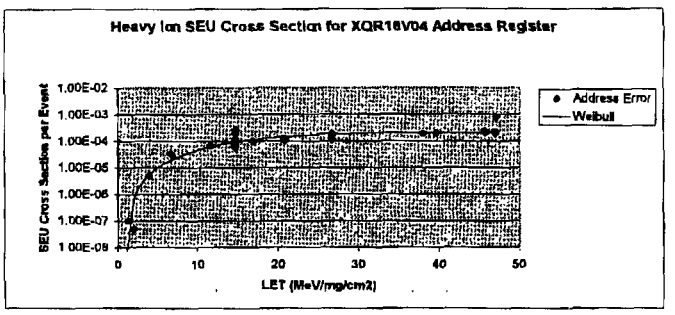

Fig. 7: Cross-section vs. effective LET for Address Errors. Saturation cross-section (σ_{sat}) is 2.1E-4 cm^2/device, L_0 is 1.0 MeVcm^2/mg, w=18 and s=2.

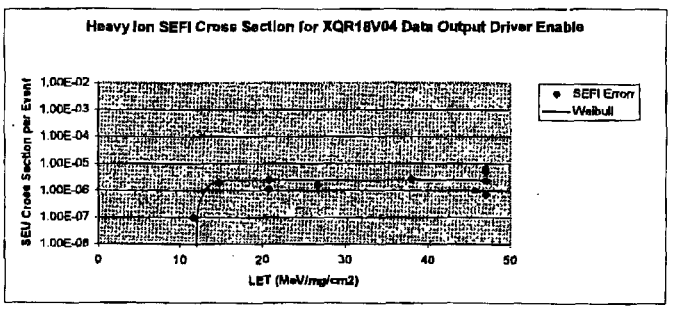

Fig. 8: Cross-section vs. effective LET for SEFI Errors. Saturation cross-section (σ_{sat}) is 2.4E-6 cm^2/device, L_0 is 11.6 MeVcm^2/mg, w=2 and s=2.

C. *Extended TID Test*

The results of the gamma dose test are shown in table 4. Configurations 2 and 3 passed the on-site functional test with 100krad total ionizing dose. This demonstrates a better than 2X increase in TID life. Tests at higher dose however, failed the functional test. The devices were subsequently allowed to anneal and tested periodically with a full AC parametric test program. The results are shown in table 5.

Table 4: Gamma dose test functional test results

Sample	Configuration	Total Dose	Pass/Fail	Test Failed
SN1	1	100 krad	Fail	3
SN4	1	300 krad	Fail	1
SN2	**2**	**100 krad**	**Pass**	-
SN7	2	200 krad	Fail	1
SN8	2	200 krad	Fail	1
SN5	2	300 krad	Fail	1
SN3	**3**	**100 krad**	**Pass**	-
SN9	3	200 krad	Fail	1
SN10	3	200 krad	Fail	1
SN6	3	200 krad	Fail	1

Table 5: AC parametric test results after anneal

Sample	Config-uration	Total Dose (krad)	Production Test Program - Pass/Fail (Anneal Hrs)		
			(24)	(48)	(168)
SN1	1	100	Fail	Fail	Fail
SN4	1	300	Fail	Fail	Fail
SN2	**2**	100	**Pass**	**Pass**	**Pass**
SN7	2	200	Fail	Not Tested	**Pass**
SN8	2	200	Fail	Not Tested	**Pass**
SN5	2	**300**	Fail	Fail	**Pass**
SN3	**3**	100	**Pass**	**Pass**	**Pass**
SN9	3	200	Fail	Not Tested	**Pass**
SN10	3	200	**Fail**	**Not Tested**	**Pass**
SN6	3	200	Fail	**Pass**	**Pass**

After 168 hours of room temperature unbiased anneal, every sample used in configuration 2 and 3 was completely restored to pre-dose functionality. The anneal test

demonstrated that at space dose rates the parts are good passed 300krad(Si) using either configuration 2 or 3.

From the test results in table 3, using a 16% duty cycle on the PROM bias effectively doubled the proton TID previously measured for these devices.

IV. Discussion

The XQR18V04 under static conditions demonstrates immunity to memory cell upset and latch-up. When in use or under dynamic operating conditions, it demonstrates error modes in the data decoder, address, and output data drivers.

When used as a configuration PROM for an SRAM based FPGA the data error rate should be included in the configuration memory upset rate of the FPGA. The address and SEFI error rates should be added to the SEFI rates of the FPGA. The error rates from continuous operation of the PROM will only make a minor contribution to the FPGA error rates. Decreasing the frequency of PROM use will make the additional error rate from the PROM negligible.

Holding the PROM in an un-biased state when not in use increases its maximum total ionizing dose to match that of the FPGA.

V. Conclusion

The XQR18V04 is a viable component for SRAM-FPGA configuration data storage in space applications.

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References

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